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# Design and Implementation of FPGA-based Systolic Array for LZ Data Compression.

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Publisher: INTECH Open Access Publisher, 2010.

Edition/Format: eBook : Document : English

Summary: In this chapter, a parallel algorithm for LZ based data compression is described by transforming a datadependent algorithm to a data independent regular algorithm. To further improve the latency, a control variable to indicate early completion is used. The.

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